

IEEE 33rd INTERNATIONAL SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS (IPFA 2026)

13th – 16th July 2026 | Marina Bay Sands Singapore

2nd CALL FOR PAPERS

IPFA 2026 is devoted to the fundamental understanding of the electrical and physical characterization techniques and associated technologies that assist in probing the nature of failures in conventional, modern and disruptive semiconductor materials, devices and systems. The Technical Program Committee is inviting papers related, but not limited to, the following areas:

IPFA will host the 2026 International ESD Workshop (IEW). More details coming soon on our webpage, stay tuned!

FAILURE ANALYSIS (FA) TRACKS

FA-1 - Sample Preparation, Metrology and Defect Characterization: Device / Advance packaging de-processing, Ion beam / TEM sample preparation, Automation of Metrology and Sample Preparation, Silicon defect inspection.

FA-2 - Electrical Fault Isolation Techniques: Photon, Laser and Electron beam-based microscopy techniques, Static and Tester based techniques, Nanoprobing, AFP, EBAC/EBIC, Next-generation backside power-rail analysis.

FA-3 - Case Studies on Fault Isolation: Application of non-destructive workflows for defect localization. Die / Board / System-level electrical FA, Electrical characterization and nanoprobing.

FA-4 - Board, System and Product Level Failure Analysis: Design for manufacturing, Test diagnostics, Embedded BIST and DFT test and diagnosis, protocol-aware testing, Test-to-Design feedback, mixed signal and analog tests, silicon failure debug by test.

FA-5 - Physical Failure Analysis Techniques: Advanced methodologies in PFA, Advanced optical/Ion beam approaches, Plasma/Laser FIB, Spectroscopy (EDX/EELS/SIMS) techniques, Scanning probe microscopy, Circuit-edits, De-layering recipe innovations, Tomography.

FA-6 - Case Studies on Physical Failure Analysis: Die / Board / System-level physical FA, Workflows, Defect exposure and characterization in silicon devices.

FA-7 - Package-Level Failure Analysis Techniques and Case Studies: Heterogenous integration/Flip-chips/Wire-bond Package FA and workflows, Non-destructive analysis including Magnetic/acoustic/ X-ray/ Lock-in thermography/ EOTPR/ Material Analysis, embedded power delivery components, wafer & panel analysis.

FA-8 - AI for FA : AI for fault detection, visual / image analytics, pattern recognition, signal processing, Deep Learning for Automated Defect Classification, Generative Models for Synthetic Failure Data Augmentation, Denoising and Super Resolution Techniques for FA.

MILESTONES	DEADLINES
Extended Abstract Submission	16 Jan 2026
Notification of Abstract Acceptance	20 Mar 2026
Full Manuscript Submission	20 Apr 2026
Final Manuscript Submission + Copyright	01 Jun 2026



RELIABILITY (REL) TRACKS

REL-1 - Transistor and Emerging Electron Devices Reliability:

- LOGIC Reliability** - Gate oxide / High-k, PBTI/NBTI, dopant effects, Self Heating in CMOS, GAA FET / CFET / Ferroelectric FET / RFSOI / HBM / DRAM / 2D material / MEOL device reliability and variability (process and stress-induced).
- MEMORY Reliability** - NVM reliability – retention, endurance and read disturb noise in PCRAM, RRAM, FeRAM, NAND Flash and STT-MRAM.
- APPLICATION Specific Reliability** - Reliability of display modules, lasers, LEDs, solar cells, CMOS image sensors, photodetectors, waveguides, silicon photonics, MEMS devices, flexible and wearable electronics and thermoelectrics.

REL-2 – Interconnect and Advanced Package Reliability: Modeling /simulation of TDDB dielectrics, Electro and stress migration, cracking/corrosion/fatigue in bond pads, wire and wafer bonds, Reliability of 3DIC/ TSV, Thermo-mechanical stress, chip-package interaction.

REL-3 – AI for Reliability & Reliability for AI: ML for prognosis & reliability. Reliability assessment for neuromorphic; in-memory computing devices and AI hardware accelerators) Telemetry and in-situ assessment of lifetime and reliability, Reliability of AI dedicated circuits.

REL-4 - Hardware Security: Semi-Invasive and Invasive Analysis for attack of encryption system and countermeasures, Counterfeit Electronics Detection, Hardware Trojan localization, Die-Level Reverse Engineering for hardware assurance (Preparation, Image Analysis, Netlist recovery)

REL-5 - High Power Electronics / Wide Bandgap Device Reliability: Reliability and Failure Analysis of GaAs, GaN HEMT, SiC and Ga₂O₃ devices, Trap-related degradation, Materials-related defect characterization, Process variability, III-V/Si integration and related case studies of failures.

REL-6 - ESD, EOS, Latch-Up: Component and system level ESD design: modeling and simulation, Novel EOS/ESD Test and Characterization Methods, ESD/EOS and radiations-triggered Latch-up issues.

IPFA Webpage



- Extended abstract and full paper** (min. of 3 pages to a max. of 6 pages including text and figures) of your original research work. Accepted abstracts will require a full manuscript (min. 4 pages) to be submitted by **20th Apr** and post-mentored final manuscripts by **1st Jun**.
- SPECIAL ISSUE JOURNAL** - High quality papers presented at IPFA 2026 will be invited to submit an extended version of their work for a **Special Issue of Microelectronics Engineering (Impact Factor 3.1)**, expected to be published in 2027, or as articles in **EDFA magazine**.

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